REMARKS

Reconsideration of the present application is requested. Claims 2, 3, 8, 9, 19 and 20 have been withdrawn from consideration. Claims 6 and 17 have been canceled without prejudice or disclaimer.

INFORMATION DISCLOSURE STATEMENT

Applicants appreciate the Examiner's consideration of the Information Disclosure Statements filed March 30, 2004 and November 3, 2005.

DRAWINGS

Applicants appreciate the Examiner's acceptance of the drawings.

PRIORITY DOCUMENTS

Applicants appreciate the Examiner's acknowledgement of Applicants' claim for foreign priority and the indication that certified copies of the priority documents have been received.

ELECTION OF SPECIES REQUIREMENT

Applicants acknowledge the withdrawal of claims 2, 3, 8, 9, 19 and 20 from consideration. Applicants also acknowledge the Examiner's indication that claim 1 is generic to all of species I-IV. As currently amended, claim 1 remains generic to all of species I-IV. Upon allowance of generic claim 1, Applicants request rejoinder of withdrawn claims 2, 3, 8, 9, 19 and 20.

PRIOR ART REJECTIONS

Rejection Under 35 U.S.C. § 102(b)

Claims 16-18, 21-25 and 28 stand rejected under 35 U.S.C. § 102(b) as allegedly anticipated by U.S. Patent No. 4,386,367 ("*Peterson*"). This rejection is respectfully traversed.

FIG. 3 of *Peterson* illustrates an embodiment of a conversion system 20. Referring to FIG. 3, alternate lines of an input image signal are received by an input latch 30. The input image signal is converted in 8 bit segments from serial to parallel form by input shift register 32. The converted input image signal data is stored into sequential storage locations of a storage device 36 in synchronization with the clock signal TDCLK. Concurrent with storing the input image signal data, image information is read from the storage device 36, and output to the output shift register 40 for conversion from parallel to serial form. The converted data is made available to the output latch 42 for subsequent transmission.

The storage of input image signal data in the storage device 36 is controlled by a write counter 50 and a write control circuit 52. The write counter 50 and the write control circuit 52 operate in accordance with a clock signal TDCLK. Information retrieval from the storage device 36 is controlled by a read counter 54 and a read control circuit 56. The read counter 54 and the read control circuit 56 operate in accordance with a second clock signal XDCLK. An address multiplexer 58 alternately selects certain write and read address signals output by the two counters 50 and 54 for application to a

storage device 36. The multiplexer 58 selects the write and read address signals based on an R/W signal generated by the write control circuit 52.

The Examiner relies upon the storage device 36 and the multiplexer 58 of *Peterson* to allegedly teach the "memory," and the "address controller," respectively, of claim 16, for example. Contrary to claim 16, however, the storage device 36 is not "configured to generate a write signal," and the multiplexer 58 is not "an address controller selectively applying the write and read addresses to the memory based on the write signal generated by the memory." As the Examiner will appreciate from review of FIG. 3 of *Peterson*, the storage device 36 of *Peterson* does not generate any signal. At most, the multiplexer 58 selectively applies write and read addresses to storage 36 in accordance with an R/W signal output from the write control circuit 52. Therefore, *Peterson* fails to disclose at least a "a memory configured to generate a write signal," and "an address controller selectively applying the write and read addresses to the memory based on the write signal generated by the memory," as required by claim 16.

For at least the foregoing reasons, claim 16 and all claims dependent there from are patentable over *Peterson*. Claims 25 and 28 are patentable over *Peterson* for at least reasons somewhat similar to those set forth above with regard to claim 16.

Rejection Under 35 U.S.C. § 102(e) – *Yugami*

The Examiner rejects claims 1, 4, 15 and 26-27 under 35 U.S.C. § 102(e) as anticipated by U.S. Patent No. 6,927,801 ("*Yugami*"). This rejection is respectfully traversed.

On page 7 of the current Office Action, the Examiner correctly recognizes that *Yugami* fails to teach or fairly suggest at least the features of claim 6, which have been incorporated into claim 1. Therefore, claim 1 is patentable over *Yugami*. Claims 15 and 26 recite features somewhat similar to those set forth in claim 1, and thus, are also patentable over *Yugami*. Claims 4 and 27 are patentable over *Yugami* at least by virtue of their dependency from claims 1 and 26, respectively.

Rejection Under 35 U.S.C. § 103 – *Yugami* and *Peterson*

The Examiner rejects claims 5-7 and 10-14 under 35 U.S.C. § 103(a) as allegedly unpatentable over *Yugami* in view of *Peterson*. This rejection is respectfully traversed. Applicants will address this rejection with regard to amended claim 1, which is believed to be patentable over *Yugami* and *Peterson*, taken singly or in combination.

The Examiner correctly recognizes that *Yugami* fails to teach or fairly suggest at least the features previously set forth in claim 6, but now set forth in claim 1. The Examiner relies upon *Peterson* to allegedly teach these features. However, as argued above with regard to claim 16, for example, multiplexer 58 is not "an address controller selectively applying the write and read addresses to the memory based on the write signal generated by the

memory." Therefore, even assuming *arguendo* that *Yugami* and *Peterson* could be combined (which Applicants do not admit), the combination still fails to teach or fairly suggest all features of amended claim 1. Therefore, claim 1 is patentable over *Yugami* and *Peterson*, taken singly or in combination. Claims 5, 7 and 10-14 are patentable at least by virtue of their dependency from claim 1.

CONCLUSION

Accordingly, in view of the above amendments and remarks, reconsideration of the objections and rejections and allowance of the pending claims is earnestly solicited.

If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number listed below.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

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By_____

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